# Technology Readiness Level (TRL) Advancement of the MSPI On-Board Processing Platform for the ACE Decadal Survey Mission

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*Abstract*— The Xilinx Virtex-5QV is a new Single-event Immune Reconfigurable FPGA (SIRF) device that is targeted as the spaceborne processor for the NASA Decadal Survey Aerosol-Cloud-Ecosystem (ACE) mission's Multiangle SpectroPolarimetric Imager (MSPI) instrument, currently under development at JPL. A key technology needed for MSPI is on-board processing (OBP) to calculate polarimetry data as imaged by each of the 9 cameras forming the instrument. With funding from NASA's ESTO[1] AIST[2] Program, JPL is demonstrating how signal data at 95 Mbytes/sec over 16 channels for each of the 9 multi-angle cameras can be reduced to 0.45 Mbytes/sec, thereby substantially reducing the image data volume for spacecraft downlink without loss of science information. This is done via a least-squares fitting algorithm implemented on the Virtex-5 FPGA operating in real-time on the raw video data stream.

The MSPI instrument development consists of three phases: Ground-MSPI, Air-MSPI, and Space-MSPI. Ground-MSPI is a ground-based camera demonstration focused on characterizing the imager optics and performance. Air-MSPI is an updated version of the ground system that was flown twice on an ER-2 aircraft in 2010. Lessons learned from the ground- and air-based demonstrations will be used in the future design of the satellite-based Space-MSPI instrument. In the first 2-years of the AIST task, the OBP algorithm has been demonstrated on a commercial Xilinx Virtex-5 FPGA-based development platform integrated with the Ground-MSPI camera system and also instantiated directly on the Air-MSPI electronics' military-grade Virtex-5 FPGA for validation in the laboratory environment. In Year 3, airborne validation of the OBP algorithm is planned with another ER-2 flight of Air-MSPI.

A related task funded in 2010 by NASA's ESTO ATI[3] Program integrates the MSPI OBP algorithm on the Virtex-5 SIRF device as a payload to the University of Michigan's M-Cubed CubeSat to gain on-orbit validation of this platform and thereby further advance the Technology Readiness Level (TRL) for MSPI and the ACE mission. This new task is called COVE (CubeSat On-board processing Validation Experiment). M-Cubed, carrying the JPL-provided COVE processor payload, has been selected for launch on the NPOESS Preparatory Project (NPP) Mission, currently scheduled on a Delta-II launch vehicle out of Vandenberg Air Force Base on October 25, 2011.

[1] Earth Science Technology Office (ESTO)
[2] Advanced Information Systems Technology (AIST)
[3] Advanced Technologies Initiatives (ATI)

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## 1 INTRODUCTION

The Multiangle SpectroPolarimetric Imager (MSPI) is an instrument concept in development at JPL to produce a highly accurate multiangle-multiwavelength polarimeter to measure cloud and aerosol properties as called for by the Aerosol-Cloud-Ecosystem (ACE) tier-2 mission concept in the Decadal Survey. This instrument has proposed 9 cameras (8-fixed and 1-gimballed), each of which must eventually process a raw video signal rate around 95 Mbytes/sec over 16-20 channels for space flight. A computationally intensive linear least-squares algorithm must also be applied to perform data reduction for video processing of the signal output from the photo-detector array. These data reductions can be performed (without sacrificing the information content of the camera product for science) based on how the calculations are implemented for

digital signal processing in the Xilinx Virtex-5FXT FPGA. The result of the on-board processing algorithm is the reduction of dozens of samples acquired during a 40-msec frame to five parameters. Averaging cross-track and along-track pixels to reduce spatial resolution achieves further data reduction. The technology under development and described here is required to enable this process to occur in real-time, with the speed necessary to keep up with the MSPI data throughput. For a complete mathematical description of the data processing algorithm, see the journal articles in *Applied Optics* [1][2]. A 2010 IEEE Aerospace Conference paper provides a concise overview of the algorithm with an emphasis on implementation details [3].

MSPI is being developed as a follow on to the Multi-angle Imaging SpectroRadiometer (MISR) [4], that has been operating since 2000 aboard NASA's Terra satellite. The first MSPI camera system developed is called LabMSPI consisting of a single 660-nm spectral band with channels having 0º and -45º polarizers, and no polarizer. LabMSPI was later upgraded to a multi-band version now known as Ground-MSPI. The spectral bands of the Ground-MSPI camera are 335, 380, 445, 470, 555, 660, 865, 935 nm where the bands at 470, 660 and 865 nm are polarimetric. At ESTF 2010 we presented on the real-time on-board processing validation of Ground-MSPI camera images [5]. Air-MSPI is customized for flight on NASA's ER-2 high altitude aircraft and successfully flew twice in 2010. In this past year under AIST funding we have integrated the OBP algorithm with Air-MSPI and performed real-time validation of camera images in the lab to achieve TRL-5. We are presently preparing for another ER-2 flight where we will validate the OBP algorithm with real-time image data to achieve TRL-6. The ATI task known as COVE builds on the AIST task development to integrate the Virtex-5 FPGA and OBP algorithm as a secondary electronics payload of a university CubeSat to further advance the TRL via low Earth orbit demonstration.

## 2 TRL DEFINITIONS

Table 1 provides the NASA Technology Readiness Level (TRL) definitions for levels 4-8 for both hardware and software descriptions. This is a collaborative and synergistic effort between the AIST and ATI tasks to advance the TRL of the hardware component (Virtex-5 FPGA) and software/firmware component (algorithm) for MSPI OBP and the ACE decadal survey mission. The AIST task began in TRL-4 with a preliminary version of the algorithm demonstrated on a prototype development board containing the FPGA. Final demonstration of TRL-4 was completed with the Ground-MSPI camera where real-time image data was essentially post-processed using this development platform. The Air-MSPI camera system provides an integrated system for TRL-5 and TRL-6 advancement of both the hardware and software components of OBP (shown in green). M-Cubed/COVE enables TRL-7 advancement of the algorithm, and potentially TRL-8 advancement of the hardware component as the Single-event Immune Reconfigurable FPGA device will be flown.

TABLE 1. NASA TRL DEFINITIONS (TRL-4 THROUGH TRL-8)

| Technology Readiness Level (TRL) | Definition | Hardware Description | Software Description |
|---|---|---|---|
| 4 | COMPONENT or breadboard validation in laboratory | A low fidelity system/component breadboard is built and operated to demonstrate basic functionality and critical test environments and associated performance predicitions are defined relative to the final operating environment. | Key, functionally critical, software components are integrated, and functionally validated, to establish interoperability and begin architecture development. Relevant Environments defined and performance in this environment predicted. |
| 5 | COMPONENT or breadboard validation in a relevant environment | A mid-level fidelity system/component brassboard is built and operated to demonstrate overall performance in a simulated operational environment with realistic support elements that demonstrates overall performance in critical areas. Performance predictions are made for subsequent development phases. | End-to-end Software elements implemented and interfaced with existing systems/simulations conforming to target environment. End-to-end software system, tested in relevant environment, meeting predicted performance. Operational Environment Performance Predicted. Prototype implementations developed. |
| 6 | SYSTEM/ SUBSYSTEM model or prototype demonstration in a relevant environment | A high-fidelity system/component prototype that adequately addresses all critical scaling issues is built and operated in a relevant environment to demonstrate operations under critical environmental conditions. | Prototype implementations of the software demonstrated on full-scale realistic problems. Partially integrate with existing hardware/software systems. Limited documentation available. Engineering feasibility fully demonstrated. |
| 7 | System prototype demonstration in space | A high fidelity engineering unit that adequately addresses all critical scaling issues is built and operated in a relevant environment to demonstrate performance in the actual operational environment and platform (ground, airborne or space). | Prototype software exists having all key functionality available for demonstration and test. Well integrated with operational hardware/software systems demonstrating operational feasibility. Most software bugs removed. Limited documentation available. |
| 8 | Actual system completed and flight qualified through test and demonstration | The final product in its final configuration is successfully demonstrated through test and analysis for its intended operational environment and platform (ground, airborne or space). | All software has been thoroughly debugged and fully integrated with all operational hardware and software systems. All user documentation, training documentation, and maintenance documentation completed. All functionality successfully demonstrated in simulated operational scenarios. V&V completed.. |

## 3 TRL SUMMARY: MSPI OBP

Table 2 shows the MSPI OBP product breakdown (system/subsystem/assembly/component) and technology level assessment for each of the key technology items that have been identified for the task. For OBP firmware/software each component gains TRL advancement based on the system in which validation occurs – Ground-MSPI camera (TRL-4), Air-MSPI camera in lab (TRL-5), Air-MSPI camera on ER-2 flight (TRL-6), M-Cubed/COVE on-orbit (TRL-7). The OBP hardware TRL advancement is tied to the grade of the FPGA device (commercial, military, SIRF/rad-hard) as well as the validation system.

TABLE 2. MSPI OBP TRL ASSESSMENT

| *Product breakdown* | | | *Technology Level Assessment* | |
|---|---|---|---|---|
| **System / Subsystem** | **Assembly** | **Component** | **Key Technology Items*** | **TRL** |
| **OBP for MSPI** | | | | **5** |
| | | | | |
| ***OBP Hardware*** | | | | |
| | Commercial Development Platform | | | **4** |
| | | Xilinx ML510 Development Board | V5FX130T, Commercial grade FPGA | 4 |
| | | Xilinx ML507 Development Board | V5FX130T, Commercial grade FPGA | 4 |
| | Ground-MSPI Camera | | | **4** |
| | | Xilinx ML507 Development Board | V5FX130T, Commercial grade FPGA | 4 |
| | AirMSPI Camera | | | **5/6** |
| | | AirMSPI Focal Plane Control Processor (FPCP) Board | V5FX70T, Military grade FPGA | **5/6** |
| | *M-Cubed/COVE* | | | |
| | | *COVE Payload Processor* | *V5FX130T, SIRF/ES (Rad-Hard) FPGA* | *8* |
| ***OBP Firmware*** | | | | |
| | Commercial Development Platform | | | **4** |
| | | IP: Multiply & Accumulate | | 4 |
| | | IP: Local Link DMA Front-End | | 4 |
| | Ground-MSPI Camera | | | **4** |
| | | IP: Multiply & Accumulate | | 4 |
| | | IP: Local Link DMA Front-End | | 4 |
| | AirMSPI Camera | | | **5/6** |
| | | IP: Multiply & Accumulate | | **5/6** |
| | *M-Cubed/COVE* | | | |
| | | *IP: Multiply & Accumulate* | | *7* |
| ***OBP Software*** | | | | |
| | Commercial Development Platform | | | **4** |
| | | uShell | | 5 |
| | | MSPI Algorithm Parameter Generation Code | | 4 |
| | | System Initialization Software | | 4 |
| | Ground-MSPI Camera | | | **4** |
| | | uShell | | 5 |
| | | MSPI Algorithm Parameter Generation Code | | 4 |
| | | System Initialization Software | | 4 |
| | AirMSPI Camera | | | **5/6** |
| | | uShell | | **5/6** |
| | | MSPI Algorithm Parameter Generation Code | | **5/6** |
| | | System Initialization Software | | **5/6** |
| | *M-Cubed/COVE* | | | |
| | | *MSPI Algorithm Parameter Generation Code* | | *7* |
| | | *System Initialization Software* | | *7* |

## 4 TRL ADVANCEMENT

### *4.1 TRL-4: Ground-MSPI in Lab*

Last year we presented validation results of the MSPI OBP algorithm running on the FPGA performing real-time data processing of raw imagery from the Ground-MSPI camera [5]. Figure 1 shows our Ground-MSPI demo system. The Ground-MSPI electronics has a two-board configuration that includes a Focal Plane Assembly (FPA) and a Data Recovery Board (DRB), each with a Spartan-3 FPGA. To demonstrate OBP of the Ground-MSPI images we simply integrated the ML507 development board (with the OBP FPGA algorithm) at the end of the image data stream.

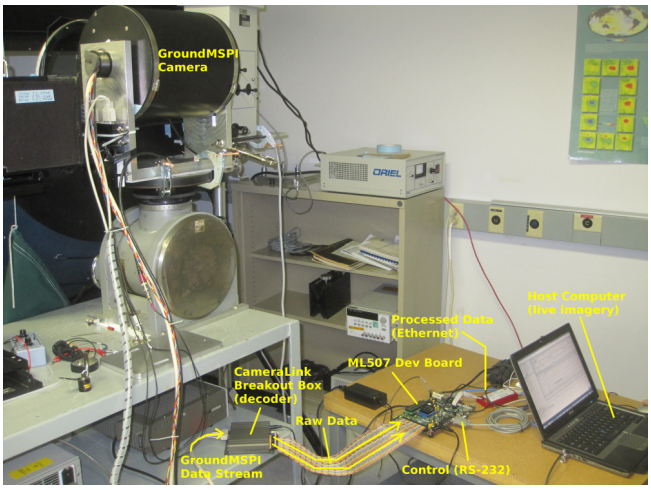



**Figure 1. The Ground-MSPI Demo System**

### *4.2 TRL-5: Air-MSPI in Lab*

The Air-MSPI Electronics has a single Focal Plane Control & Processing (FPCP) board with a military grade Virtex-5FX70T FPGA to enable OBP path-to-flight for ACE (Figure 2). For this demonstration the OBP algorithm is integrated with the rest of the Air-MSPI operational FPGA code for execution on the single device.

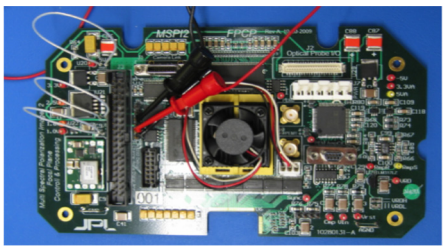


**Figure 2. Air-MSPI FPCP Board. The Virtex-5 FPGA is in the center of the board under the fan.**

Air-MSPI input data to the MSPI OBP hardware requires a custom data acquisition frontend. The CameraLink data capture logic from the Ground-MSPI demonstration is replaced with direct data capture from the FPA controller core. The processed output data is sent to an off-FPGA on-board CameraLink encoder for streaming to recording units (Figure 3).

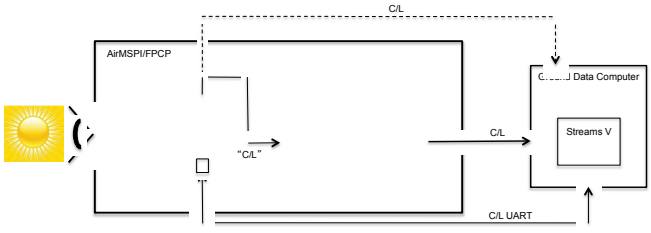



**Figure 3. Air-MSPI Demo System Diagram**

Laboratory-based validation of Air-MSPI OBP is in progress (Figure 4). Assessment of TRL-5 advancement is expected by June 2011.

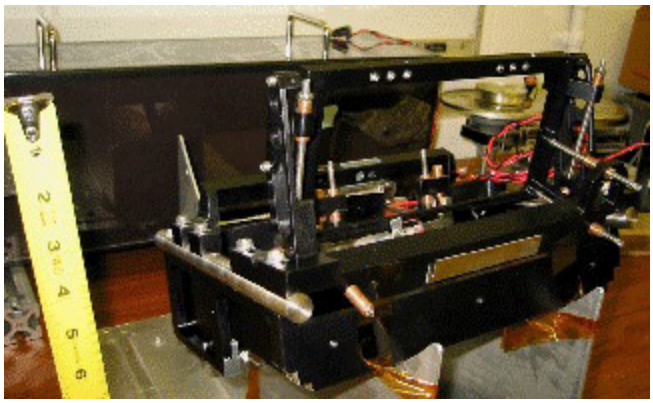


**Figure 4. The Air-MSPI Camera in the lab**

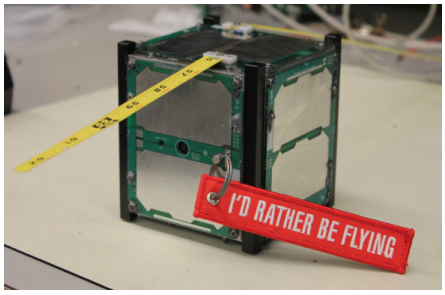
### *4.3 TRL-6: Air-MSPI on ER-2*

Preparations are underway for an Air-MSPI ER-2 flight in July/August 2011. Validation of the OBP results of this flight demonstration will be performed in order to assess TRL-6 advancement by the time the AIST task concludes in Feb. 2012.

### *4.4 M-Cubed/COVE: Beyond TRL-6*

COVE is an 18-month funded task to develop the flight-ready U. Michigan M-Cubed CubeSat (Figure 5) with an integrated JPL electronics payload (Figure 6) [6]. M-Cubed's primary payload is an OmniVision 2 MegaPixel CMOS camera (Figure 7) that will take quality color images of the Earth from Low Earth Orbit (LEO) and save them to a Taskit Stamp9G20 microprocessor. The secondary payload provided by JPL provides a data processing platform for on-orbit validation of the MSPI OBP algorithm running on the Virtex-5 FPGA.

**Figure 5. U.Michigan's M-Cubed CubeSat (Engineering Model), 10 x 10 x 10 cm**



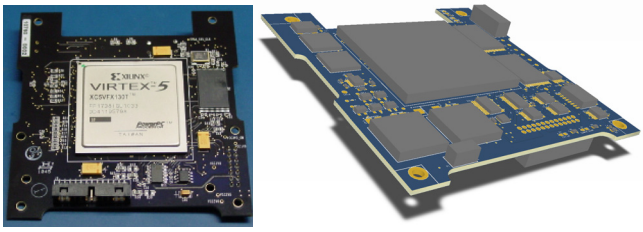




**Figure 6. JPL's COVE Payload Processor, Engineering Model (Left), Flight Model Layout (Right)**

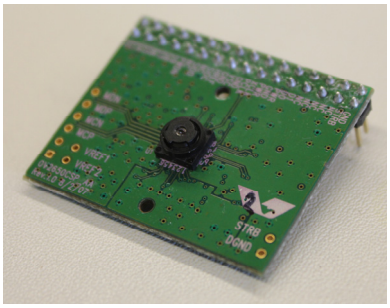


**Figure 7. M-Cubed Camera Payload [7]**

The COVE payload processor, integrated on the M-Cubed CubeSat, has been selected for launch on the NPOESS Preparatory Project (NPP) Mission. This selection was part of the Space Operations Mission Directorate's (SOMD) 2010 CubeSat Launch Initiative [8]. The NPP satellite will be launched from the Western Range at Vandenberg Air Force Base from SLC-2, California, by a Boeing Delta II-7920-10 launch vehicle. The NPP mission will be launched into an 824 km circular, sun-synchronous orbit with a 10:30 a.m. local-time descending node crossing. NPP is currently schedule for launch on October 25, 2011.

## 5 CONCLUSION

MSPI and other future JPL science instruments will rely on the hardware acceleration provided by FPGA embedded technology to meet their on-board processing (OBP) requirements. The 3-year AIST task has provided a solid platform to advance MSPI OBP development from TRL-4 to TRL-6 with demonstration on the Ground-MSPI and Air-MSPI camera systems in the laboratory and the upcoming Air-MSPI ER-2 flight demo. The highly anticipated release of the space-grade Xilinx Virtex-5 FXT130 is manufactured as a Single event Immune Reconfigurable FPGA (SIRF), and it is this device that is baselined for the future Space-MSPI camera system targeted for the ACE Decadal Survey Mission [9]. Rapid advancement beyond TRL-6 can be accomplished from the low-cost capability of CubeSats to carry small payloads such as the Virtex-5 SIRF device, into LEO. This is the goal of the ATI-funded task called COVE.

## ACKNOWLEDGEMENTS

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## BIOGRAPHY

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